

Command and control circuitry **130** controls the operation of memory **100** in response to control signals received on control lines **135** from a processor **140** or other memory controller during read, write, refresh, and erase operations. Command and control circuitry **130** includes a refresh circuit for periodically refreshing the data stored on [floating gate transistor or other floating electrode memory cells **110**] the memory cells **110**. Voltage control **150** provides appropriate voltages to the memory cells during read, write, refresh, and erase operations. Memory **100**, as illustrated in Figure **1**, has been simplified for the purpose of illustrating the present invention and is not intended to be a complete description. Only the substantial differences between DEAPROM memory **100** and conventional DRAM and flash EEPROM memories are discussed below.

The paragraph beginning at page 16, line 21 is amended as follows:

The lower barrier energy Φ_{cl} and increased tunneling current also advantageously reduces the voltage required for writing and erasing [the floating gate transistor memory cells **110**] the memory cells **110**. For example, conventional polysilicon floating gate transistors typically require complicated and noisy on-chip charge pump circuits to generate the large erasure voltage, which typically far exceeds other voltages required on the integrated circuit. The present invention allows the use of lower erasure voltages that are more easily provided by simpler on-chip circuits. Reducing the erasure voltage also lowers the electric fields, minimizing reliability problems that can lead to device failure, and better accommodating downward scaling of device dimensions. In one embodiment, the barrier energy Φ_{cl} is selected, as described above, to obtain an erase voltage of less than the 12 Volts required by typical EEPROM memory cells.

The paragraph beginning at page 17, line 21 is amended as follows:

According to one aspect of the present invention, the data stored on the [DEAPROM floating gate memory cell **110**] memory cell **110** is periodically refreshed at an interval that is shorter than the data charge retention time. In one embodiment, for example, the data is refreshed every few seconds, such as for an embodiment having a high temperature retention time of approximately 40 seconds for $\Phi_{cl} = 1.08$ eV. The exact refresh rate can be

experimentally determined and tailored to a particular process of fabricating the DEAPROM. By decreasing the data charge retention time and periodically refreshing the data, the write and erase operations can be several orders of magnitude faster, as described above with respect to Figure 7.

The paragraph beginning at page 18, line 13 is amended as follows:

In Figure 9B, the [DEAPROM memory cell 110 according to the present invention] memory cell 110 according to the present invention is a DEAPROM memory cell that includes floating gate FET 200, having source 205 coupled to a ground voltage or other reference potential. Data is stored as charge on floating gate 215 by providing a control voltage on control line 920 and a write voltage on data line 925 for hot electron injection or Fowler-Nordheim tunneling. This is similar to conventional EEPROM techniques, but advantageously uses the reduced voltages and/or a shorter write time of the present invention.

The paragraph beginning at page 18, line 20 is amended as follows:

The DEAPROM memory cell [110] can be smaller than the DRAM memory cell of Figure 9A, allowing higher density data storage. The leakage of charge from floating gate 215 can be made less than the reverse-bias junction leakage from storage capacitor 905 of the DRAM memory cell by tailoring the barrier energy Φ_{G1} according to the techniques of the present invention. Also, the DEAPROM memory cell advantageously uses the large transconductance gain of the floating gate FET 200. The conventional DRAM memory cell of Figure 9A provides no such gain; it is read by directly transferring the data charge from storage capacitor 905. By contrast, the DEAPROM memory cell [110] is read by placing a read voltage on control line 920, and detecting the current conducted through FET 200, such as at data line 925. The current conducted through FET 200 changes significantly in the presence or absence of charge stored on floating gate 215. Thus, the present invention advantageously provides an large data signal that is easy to detect, unlike the small data signal provided by the conventional DRAM memory cell of Figure 9A.

The paragraph beginning at page 19, line 11 is amended as follows:

For an illustrative example, but not by way of limitation, a minimum-sized FET having $W/L=1$, can yield a transconductance gain of approximately $71 \mu\text{A/Volt}$ for a typical process. In this illustrative example, sufficient charge is stored on floating gate **215** to change the effective threshold voltage V_T by approximately 1.4 Volts, thereby changing the current I_{DS} by approximately 100 microamperes. This significant change in current can easily be detected, such as by sampling or integrating over a time period of approximately 10 nanoseconds, for example, to obtain a detected data charge signal of 1000 fC. Thus, the DEAPROM memory cell **[110]** is capable of yielding a detected data charge signal that is approximately an order of magnitude larger than the typical 30 fC to 100 fC data charges typically stored on DRAM stacked or trench capacitors. Since DEAPROM memory cell **[110]** requires a smaller capacitance value than a conventional DRAM memory cell, DEAPROM memory cell **[110]** can be made smaller than a conventional DRAM memory cell. Moreover, because the CMOS-compatible DEAPROM storage capacitor is integrally formed as part of the transistor, rather than requiring complex and costly non-CMOS stacked and trench capacitor process steps, the DEAPROM memory of the present invention should be cheaper to fabricate than DRAM memory cells, and should more easily scale downward as CMOS technology advances.

The paragraph beginning at page 21, line 24 is amended as follows:

In another embodiment plasma-enhanced molecular beam epitaxy (PEMBE) is used to form a GaN or GaAlN floating gate **215**, for example, by using electron cyclotron resonance (ECR) plasma during molecular beam epitaxy (MBE). The background pressure in the MBE chamber is typically less than 10^{-10} torr. Ga flux (e.g., 99.99999% pure) is supplied by a conventional Knudsen effusion cell. The semiconductor substrates **230** are heated to a temperature of approximately 850 degrees Celsius, and exposed to a nitrogen plasma (e.g., 35 Watt plasma power level) to clean the surface of the substrate **230** and form a thin AlN layer thereupon. The temperature is then lowered to approximately 550 degrees Celsius for growth of a thin (e.g., 300 Å) GaN buffer layer (e.g., using 20 Watt plasma power level for growth in a low